What is claimed is:

[Claim 1] 1. A frequency synthesizer comprising:

a phase detector for generating an output according to a difference of a reference input and a feedback input;

an oscillator coupled to the phase detector, the oscillator capable of outputting a variable frequency signal in response to a control input;

a first divider module for generating the feedback input, the first divider module comprising a first fractional divider coupled to the oscillator for dividing a frequency of the variable frequency signal by a first time-varying value;

a second divider module for generating the reference input, the second divider module comprising a second fractional divider for dividing a frequency of a reference signal by a second time-varying value.

[Claim 2] 2. The frequency synthesizer of claim 1 further comprising a loop filter coupled between the phase detector and the oscillator for removing high frequency components of the output of the phase detector.

[Claim 3] 3. The frequency synthesizer of claim 1 wherein the oscillator is a voltage-controlled oscillator or a current-controlled oscillator.

[Claim 4] 4. The frequency synthesizer of claim 1 wherein the first divider module further comprises a first divider coupled to the first fractional divider for dividing a frequency of an output signal of the first fractional divider.

[Claim 5] 5. The frequency synthesizer of claim 4 wherein the first divider is a first integer divider.

[Claim 6] 6. The frequency synthesizer of claim 5 wherein the first integer divider is capable of dividing the frequency of the output signal of the first fractional divider by a first integer power of 2.

[Claim 7] 7. The frequency synthesizer of claim 1 wherein the second divider module further comprises a second divider coupled to the second fractional divider for dividing a frequency of an output signal of the second fractional divider.

[Claim 8] 8. The frequency synthesizer of claim 7 wherein the second divider is a second integer divider.

[Claim 9] 9. The frequency synthesizer of claim 8 wherein the second integer divider is capable of dividing the frequency of the output signal of the second fractional divider by a second integer power of 2.

[Claim 10] 10. The frequency synthesizer of claim 1 further comprising an output divider coupled to the oscillator for dividing the frequency of the variable frequency signal generated by the oscillator.

[Claim 11] 11. The frequency synthesizer of claim 10 wherein the output divider is an output integer divider.

[Claim 12] 12. The frequency synthesizer of claim 11 wherein the output integer divider is capable of dividing the frequency of the variable frequency signal generated by the oscillator by a third integer power of 2.

[Claim 13] 13. The frequency synthesizer of claim 12 wherein the first divider module further comprises a first integer divider coupled to the first fractional divider for dividing a frequency of an output signal of the first fractional divider by a first integer power of 2, the second divider module further comprising a second integer divider coupled to the second fractional divider for dividing a frequency of an output signal of the second fractional divider by a second integer power of 2.

[Claim 14] 14. The frequency synthesizer of claim 13 further comprising means for calculating the three integer powers of two by subtracting a second exponent value from a first exponent value and adding a first frequency range indicator exponent value for generating a sum.

[Claim 15] 15. The frequency synthesizer of claim 14 further comprising means for applying the sum to the first integer divider and applying zero to the output integer divider and applying the first frequency range indicator exponent value to the second integer divider when the sum is nonnegative.

[Claim 16] 16. The frequency synthesizer of claim 14 further comprising means for applying an absolute value of the sum to the output integer divider and applying zero to the first integer divider and applying the first frequency range indicator exponent value to the second integer divider when the sum is negative.

[Claim 17] 17. The frequency synthesizer of claim 14 further comprising:

means for determining whether to update the exponent values.

[Claim 18] 18. The frequency synthesizer of claim 14 further comprising:

means for generating an exponent value according to the number of left-shifts required to shift a divider control word within a floating-point register until a plurality of bits fall within a preferred range.

[Claim 19] 19. The frequency synthesizer of claim 14 further comprising:

means for storing the first exponent value and the second exponent value for subsequent cycles.

[Claim 20] 20. The frequency synthesizer of claim 14 further comprising:

means for generating the first frequency range indicator exponent value according to a frequency measurement of the reference signal.

[Claim 21] 21. The frequency synthesizer of claim 14 further comprising:

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means for generating a first floating-point significand by
 shifting a first divider control word according to the first
 exponent value;
means for generating a second floating-point significand by
 shifting a second divider control word according to the second
 exponent value.
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[Claim 22] 22. The frequency synthesizer of claim 21 further comprising means for multiplying the first divider control word by a second frequency range indicator exponent value.

[Claim 23] 23. The frequency synthesizer of claim 21 further comprising means for checking whether the floating-point significands are within an allowed range.

[Claim 24] 24. The frequency synthesizer of claim 21 further comprising means for checking whether the floating-point significands differ from the floating-point significands in the previous cycle by more than a change tolerance.

[Claim 25] 25. The frequency synthesizer of claim 21 further comprising means for checking whether the floating-point significands have overflowed during shifting.

[Claim 26] 26. The frequency synthesizer of claim 21 further comprising a first quantizer coupled to the first floating-point register for quantizing the first floating-point significand, and a second quantizer coupled to the second floating-point register for quantizing the second floating-point significand.

[Claim 27] 27. The frequency synthesizer of claim 26 wherein the quantizers are delta-sigma quantizers.

[Claim 28] 28. The frequency synthesizer of claim 27 wherein the delta-sigma quantizers are of second order.

[Claim 29] 29. The frequency synthesizer of claim 18 further comprising means for outputting an unlock signal when the exponent values have changed.

[Claim 30] 30. The frequency synthesizer of claim 29 further comprising means for generating a mute signal in response to the unlock signal.

[Claim 31] 31. The frequency synthesizer of claim 1 further comprising a frequency doubler for increasing a frequency of an input clock, and a multiplexer having a first input coupled to the input clock and a second input coupled to the output of the frequency doubler and an output coupled to the first fractional divider and a selector input for selecting which input to output to the first fractional divider.

[Claim 32] 32. The frequency synthesizer of claim 1 wherein the fractional dividers are fractional-N dividers.

[Claim 33] 33. A method for synthesizing an output signal having a frequency proportional to a frequency of an input signal comprising following steps:

(a) quantizing a first floating-point significand to generate a first time-varying value and a second floating-point significand to generate a second time-varying value;
(b) generating an output according to a difference of a reference input and a feedback input;
(c) outputting the variable frequency signal in response to a control input;
(d) dividing a frequency of the variable frequency signal by the first time-varying value; and

(e) dividing a frequency of the reference signal by the second time-varying value.

[Claim 34] 34. The method of claim 33 further comprising removing high frequency components of the output generated according to the difference of the reference input and the feedback input.

[Claim 35] 35. The method of claim 33 further comprising step (f): dividing a frequency of an output signal generated by dividing the frequency of the variable frequency signal.

[Claim 36] 36. The method of claim 35 wherein step (f) is performed by dividing the frequency of the output signal by a first integer power of 2.

[Claim 37] 37. The method of claim 33 further comprising step (g): dividing a frequency of an output signal generated by dividing the frequency of the reference signal.

[Claim 38] 38. The method of claim 37 wherein step (g) is performed by dividing the frequency of the output signal by a second integer power of 2.

[Claim 39] 39. The method of claim 33 further comprising step (h): dividing the frequency of the variable frequency signal to generate the synthesized output signal.

[Claim 40] 40. The method of claim 39 wherein step (h) is performed by dividing the frequency of the variable frequency signal by a third integer power of 2.

[Claim 41] 41. The method of claim 40 further comprising following steps:

(f) dividing a frequency of an output signal generated by dividing the frequency of the variable frequency signal by a first integer power of 2; and

(g) dividing a frequency of an output signal generated by dividing the frequency of the reference signal by a second integer power of 2.

[Claim 42] 42. The method of claim 41 further comprising calculating the three integer powers of two by subtracting a second exponent value from a first exponent value and adding a first frequency range indicator exponent value for generating a sum.

[Claim 43] 43. The method of claim 42 further comprising applying the sum to the first integer power, applying zero to the third integer power, and applying the first frequency range indicator exponent value to the second integer power when the sum is nonnegative.

[Claim 44] 44. The method of claim 42 further comprising applying an absolute value of the sum to the third integer power, applying zero to the first integer power, and applying the first frequency range indicator exponent value to the second integer power when the sum is negative.

[Claim 45] 45. The method of claim 42 further comprising determining whether to update the exponent values.

[Claim 46] 46. The method of claim 42 further comprising generating an exponent value according to the number of left-shifts required to shift a divider control word until a plurality of bits fall within a preferred range.

[Claim 47] 47. The method of claim 42 further comprising storing the first exponent value and the second exponent value for subsequent cycles.

[Claim 48] 48. The method of claim 42 further comprising generating the first frequency range indicator exponent value according to a current frequency measurement of the reference signal.

[Claim 49] 49. The method of claim 42 further comprising:

generating the first floating-point significand by shifting a first divider control word according to the first exponent value; and

generating the second floating-point significand by shifting a second divider control word according to the second exponent value.

[Claim 50] 50. The method of claim 49 further comprising multiplying the first divider control word by a second frequency range indicator exponent value.

[Claim 51] 51. The method of claim 49 further comprising checking whether the floating-point significands are within an allowed range.

[Claim 52] 52. The method of claim 49 further comprising checking whether the floating-point significands differ from the floating-point significands in the previous cycle by more than a change tolerance.

[Claim 53] 53. The method of claim 49 further comprising checking whether the floating-point significands have overflowed during shifting.

[Claim 54] 54. The method of claim 46 further comprising outputting an unlock signal when the exponent values are being recalculated.

[Claim 55] 55. The method of claim 54 further comprising generating a mute signal in response to the unlock signal.

[Claim 56] 56. The method of claim 33 further comprising increasing a frequency of an input clock, and selecting the input clock or the input clock with increased frequency to apply as the reference input.